Statistical analysis of alignment and performance for chip-to-chip communication

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Abstract

Using capacitive-based chip-to-chip signaling in large-scale systems offers an interesting tradeoff between design and packaging complexity versus power consumption and performance. Placing chips together in close proximity offers low energy per-bit costs and high I/O density, and therefore enables off-chip bandwidth levels far beyond those offered by traditional packaging and I/O technologies. Much of the previous published work on capacitive Proximity I/O has focused on mechanical methods for accurate chip alignment. In this paper we discuss some system design considerations unique to Proximity I/O. We analyze the pad's signal which is placed at different levels and different frequencies. We simulate the signal data of two of pads with overlapping area ranging from HFSS 0% (completely non-overlapping) to 100% (complete overlaping) and frequency from 1 GHz to 10 GHz signal. The signal-to-noise ratios are obtained and models are established. The objective is to investigate the level position and frequency which results in the best signal.

Keyword: capacitive-based, SNR, differential signal